Acceleration of a production Solar MHD code with Fortran standard parallelism: From OpenACC to do concurrent

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Supported by: **INSEP** NASA



The Thirteenth International Workshop on Accelerators and Hybrid Emerging Systems (AsHES)

Outline

Accelerated Computing Directives and Standard Parallelism
 Previous Implementations ● The MAS Code
 From OpenACC to Do Concurrent **Performance** Summary and Future Outlook



Why Accelerated Computing?

- *Overall* performance
 FLOP/s
 - Memory Bandwidth
 - Specialized hardware (e.g. ML/DL tensor cores)
- W Compact performance
 - In-house workstations
 - Reduce HPC real estate
 - - Lower energy use
 - Save money





Directives

- Special comments that direct/allow the compiler to generate code that the base language does not support (e.g. parallelism, GPU-offload, data movement, etc.)
- Can produce single source code base for multiple (Ψ) targets (GPU, Multi-core CPU, FPGA, etc.)
- Use Low-risk can ignore directives and compile as before
- W Vendor-independent (NVIDIA, AMD GCN, Intel, GCC, Cray, Flang, etc.)
- Great for rapid development and accelerating (Ψ) legacy codes
- **W** Two major directive APIs for accelerated computing: **OpenACC** and **OpenMP**





!\$omp target enter data map(to:x) map(alloc:y) \$ somp target teams distribute parallel do do i=1, ny(i) = a * x(i) + benddo !\$omp end target teams distribute parallel do !\$omp target exit data map(delete:x) map(from:y)

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Openace

More Science, Less Programming

!\$acc enter data copyin(x) create(y)

y(i) = a * x(i) + b

!\$acc exit data delete(x) copyout(y)

Fortran Standard Parallelism: Do Concurrent

- Introduced in ISO Standard Fortran 2008 ψ
- Indicates loop can be run with **out-of-order** Ψ) execution
- W Can be hint to the compiler that loop may be parallelizable
- Ψ No current support for reductions, atomics, device selection, conditionals, etc.
- Fortran 202X (2023) specification will add reductions



	h . t	Compiler	Version	DO CONCURRENT parallelization sup
	(mult) (nvfortran	≥ 20.11	CPU and GPU with -stdpar
899	ortran	ifort/ifx	≥ 19.1 ≥ 23.0	CPU with -fopenmp CPU and GPU with -fopenmp-target
0.8.0	accounts: gricker: (Same	gfortran	≥9	CPU with -ftree-parallelize-loop

s=<#Threads>

-do-concurrent

port

Directives vs. Standard Parallelism

Why use Fortran standard parallelism instead of directives?

- Use Longevity (ISO)
- Use Lower code footprint
- Use unfamiliar to domain scientists
- For accelerated computing, directives are currently more portable (may change)

These reasons also apply to codes that already use directives



Original Non-Parallelized Code

```
do k=1, np
  do j=1, nt
    do i=1,nrm1
      br(i,j,k) = (phi(i+1,j,k)-phi(i,j,k))*dr i(i)
    enddo
 enddo
enddo
```

!\$acc enter data copyin(phi,dr i) !\$acc enter data create(br) !\$acc parallel loop default(present) collapse(3) async(1) do k=1, np do j=1, ntdo i=1,nrm1 br(i,j,k) = (phi(i+1,j,k)-phi(i,j,k))*dr i(i)enddo enddo enddo !\$acc wait !\$acc exit data delete(phi,dr i,br)

do concurrent (k=1:np,j=1:nt,i=1:nrm1) br(i,j,k) = (phi(i+1,j,k)-phi(i,j,k))*dr i(i)enddo

OpenACC Parallelized Code



Previous Implementations

We have previously tested replacing OpenACC with DC in a small surface diffusion tool and in our medium-sized potential field solver code

The number of OpenACC directives were substantially or completely removed while Ψ maintaining similar performance

Stulajter, et. al. "Can Fortran's `do concurrent' Replace Directives for Accelerated Computing?" Lecture Notes in Computer Science, 13194, 3-21. Springer, Cham. (2021)



github.com/predsci/POT3D https://developer.nvidia.com/blog/using-fortranstandard-parallel-programming-for-gpu-acceleration





Here, we apply DC to our large-scale production code:



The MAS Code



AGNETOHUOROOUNAMIC Algorithm Outside A sphere

Purpose: General-purpose simulations of the corona and heliosphere for use with solar physics and space weather research

Model: Spherical 3D resistive thermodynamic MHD equations.

Algorithm: Implicit and explicit time-stepping with finite-difference stencils. Implicit steps use sparse matrix preconditioned iterative solver Highly memory bandwidth bound!

Code: ~70,000 lines of Fortran

Parallelism: MPI + OpenACC + StdPar



MAS OpenACC Implementation

Basic Loop



!\$acc kernels default(present) y(:,:) = a*x(:,:) + y(:,:)!\$acc end kernels



Reductions

CPU↔GPU Data transfers

"y" is allocated and initialized on CPU. **!\$acc enter data copyin (y)** (Can now use "y" in OpenACC regions) (CPU version of "y" updated for I/O, etc.) !\$acc update self (y) !\$acc exit data delete(y) (Free up GPU memory)

OpenACC

sum(i) = sum(i) + y(i,j)

MAS OpenACC Implementation Cont.

Use multiple GPUs on one or more compute nodes



call MPI Comm split type (MPI COMM WORLD, MPI COMM TYPE SHARED, & 0,MPI INFO NULL, comm shared, ierr) call MPI Comm rank (comm shared, iprocsh, ierr) !\$acc set device num(iprocsh) !Assumes #GPUs/Node = #MPIranks/Node

Use GPU data directly with MPI calls (CUDA-aware MPI)*

!\$acc host_data use_device(y) if present call MPI Allreduce (MPI IN PLACE, y, n, MPI DOUBLE, & MPI SUM, MPI COMM WORLD, ierr)

!\$acc end host data













	# of lines
	997
	320
	34
	12
	6
	6
	1
	82
e types)	02
	1458

MAS OpenACC Implementation Cont: Performance Check

A roofline analysis shows how well given hardware is being utilized compared to the theoretical maximum for the given code







MAS OpenACC to Do Concurrent

- W Multiple versions based on these considerations:
- Avoid code refactoring (or not)
- W Adhere to ISO 2018 Fortran Standard (or not)
 - Data affinity statements (part of specification) not used as they are not currently supported by some compilers (e.g. GCC)

Using 202X preview & special features (or not)

- DC Reduction clause (nvfortran only)
- OpenACC directives within DC loops
- Use Comparison Less OpenACC directives vs. performance loss
 - Unified managed memory vs. manual memory management

	Code	Code description and	Total	\$acc
	Version	nvfortran GPU compiler flags	Lines	Lines
	0: CPU	Original CPU-only version	69874	Ø
		Original OpenACC		
	1: A	implementation	73865	1458
		-acc=gpu -gpu=cc80		
		OpenACC for DC-incompatible		
		loops and data management,		
•	2: AD	DC for remaining loops	71661	540
		-acc=gpu -stdpar=gpu		
		-gpu=cc80, nomanaged		
		OpenACC for DC-incompatible		
		loops, DC for remaining loops,	-10.00	1.0
	3: ADU	Unified memory	71269	162
		-acc=gpu -stdpar=gpu		
		-gpu=cc80, managed		
		OpenACC for for functionality		
		, DC2X for remaining loops,	709/9	
	4: AD2XU	Unified memory	/0868	55
		-acc=gpu -stdpar=gpu		
*		some code modifications		
<u>`</u>		Unified memory		
	5: D2XU	-st dpar=gpu _gpu=gg80	68994	Ø
		-Minline=reshape.name.s2c.		
*		boost, interp. c2s, sv2cv		
		DC2X for all loops.		
		some code modifications.		
		OpenACC for data management		
	6: D2XAd	-acc=qpu -stdpar=qpu	71623	277
1		-qpu=cc80, nomanaged		
		-Minline=reshape, name:s2c,		
		boost, interp, c2s, sv2cv		

SUMMARY OF ALL MAS CODE VERSIONS DEVELOPED AND TESTED.

Code 2 [AD]

- Start with Fortran 2018 specification compliance; no unified managed memory; no refactoring
- W No DC reduction support in current standard, so array reduction code would need refactoring

Functions/routines inside loops:

- DC requires they are "pure"
- Even so, nvfortran does not currently support them, so need OpenACC routine directives
- W Removing kernels used for array syntax and intrinsics (e.g. MINVAL) would need refactoring

```
!$acc parallel default(present)
!$acc loop collapse(2)
do j=1,n2
  do i=1,n1
!$acc atomic update
    sum0(i) = sum0(i) + array(i, j) * ...
  enddo
enddo
!$acc end parallel
```

module c2s_interface !\$acc routine(c2s) seq interface pure subrouti use number implicit no real(r_typ) real(r typ) end subroutin end interface end module

!\$acc kernels default(present) min_field_val_local=MINVAL(field,mask) !\$acc end kernels

ne	e c2s (x,y,z,r,t,p)
ty	/pes
ne	e
,	<pre>intent(in) :: x,y,z</pre>
,	<pre>intent(out) :: r,t,p</pre>
e	c2s

Code 2

- Previous DC results show using unified managed memory (UM) can reduce performance, so we leave OpenACC data movement directives
- W Kernel fusion (OpenACC) parallel regions) and asynchronous computation (OpenACC async clause) are not available in DC
- ♥ Code 2 [AD]: **OpenACC** for DC-incompatible loops and data management **DC** for all remaining loops



ECONS 2000 (seconds) 1500 HL 1000	One A100 GPU Image: Total of the state of t	(over 4 runs 1486.2	
Sock Mall Clock Mall Clock	Original STDPAR + Min ACC Original (managed)	STDPAR + ACC (no managed	
Code Version	Code description and nvfortran GPU compiler flags Original OpenACC	Total Lines	\$acc Lines
1: A 2: AD	-acc=gpu -gpu=cc80 OpenACC for DC-incompatible loops and data management, DC for remaining loops -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged	71661	540

Code 3 [ADU]

- W Here, activate NVIDIA unified managed memory (UM) allowing removal of OpenACC data directives
- Can't remove all OpenACC data ψ) directives:
 - declare in function calls
 - Derived-type structures in OpenACC loops when using default (present)
- Code 3 [ADU]: ψ) **OpenACC** for DC-incompatible loops, DC for all remaining loops, Unified managed memory





Code	Code description and	Total	\$acc
Version	nvfortran GPU compiler flags	Lines	Lines
2: AD	OpenACC for DC-incompatible loops and data management, DC for remaining loops -acc=gpu -stdpar=gpu	71661	540
3: ADU	OpenACC for DC-incompatible loops, DC for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80,managed	71269	162

Developer View With Unified Memory Unified Memory

allocate (a%r(nrm1,nt,np)) allocate (a%t(nr,ntm1,np)) allocate (a%p(nr,nt,npm1))

\$acc enter data create(a)

Code 4 [AD2XU]

- W Here, we use the Fortran 202X preview implementation in nvfortran
- **DC** reduction clause
- W No array reductions, but can use **OpenACC** atomics in DC loop
- W Able to remove most data clauses as all loops using derived types are now DC
- Some OpenACC directives remain:
 - atomic, declare, update, set device num, routine, kernels
- **W** Code 4 **[AD2XU]**: **OpenACC** for functionality, DC 202X for all loops, **Unified managed memory**

do concurrent (k=2:npm1 reduce(+:sum0)) sum0=sum0+a(2,k)*dph(k)*pl_1*τwo enddo

do concurrent (j=1:n2,i=1:n1) !\$acc atomic update sum0(i) = sum0(i) + array(i, j) * ... enddo

Code	Code description and	Total	\$acc
Version	nvfortran GPU compiler flags	Lines	Lines
3: ADU	OpenACC for DC-incompatible loops, DC for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80.managed	71269	162
4: AD2XU	OpenACC for for functionality , DC2X for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80,managed	70868	55

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Code 5 [D2XU]

- W Here, we allow minor code refactoring
- W Replaced kernels with expanded DC loops
- W Array reduction loops modified to avoid **atomic**
- W Removed set device num by using BASH launching script (OpenMPI-based) mpiexec -np <#> ./launch.sh ./mas
- Use nvfortran flags to in-line routines, explicitly listing routines that can't be automatically in-lined
- Can eliminate duplicate CPU-only (Ψ)
- ♥ Code 5 [D2XU]: DC 202X for all loops, Some code refactoring, Unified managed memory



launch.sh

#!/bin/bash Assume 1 GPU per MPI local rank Set device for this MPI rank: export CUDA_VISIBLE_DEVICES=" \$OMPI COMM WORLD LOCAL RANK" # Execute code: exec \$*

utines	Code Version	Code description and nvfortran GPU compiler flags	Total Lines	\$acc Lines
AE SCIENCE	4: AD2XU	, DC2X for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80.managed	70868	55
PADGRAMA	5: D2XU	<pre>DC2X for all loops, some code modifications, Unified memory -stdpar=gpu -gpu=cc80 -Minline=reshape,name:s2c, boost,interp,c2s,sv2cv</pre>	68994	Ø

do concurrent (j=1:n2) reduce(+:tmp)

Code 6 [D2XAd]

Spoiler alert: Unified Managed Memory currently results in a nontrivial performance hit, especially across many MPI ranks

Here, we take Code 5, but add back in (in minimal form) OpenACC data directives

Result is minimal number of directives, while retaining original performance

 Code 6 [D2XAd]: DC 202X for all loops, Some code refactoring, OpenACC for data management



Code	Code description and	Total	\$acc
Version	nvfortran GPU compiler flags	Lines	Lines
5: D2XU	<pre>DC2X for all loops, some code modifications, Unified memory -stdpar=gpu -gpu=cc80 -Minline=reshape,name:s2c, boost_interp.c2s_sv2cv</pre>	68994	Ø
6: D2XAd	DC2X for all loops, some code modifications, OpenACC for data management -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged -Minline=reshape, name:s2c, boost, interp, c2s, sv2cv	71623	277

MAS Test Case and Computational Environment

- Medium-sized production thermodynamic coronal relaxation
- W 36 million cells, 24 minutes physical time – Can fit on single 40GB GPU
- DC has no effect on performance for CPU-only MPI runs:

	HN-S	UNDARIE	s SD	SC
# CPUs x Mode	el	(2x)	EPYC 7742	
# Total Cores		128	(we use 64)	
Peak FLOP/s		7.0 TFLOP/s		
Memory		256 GB		
Total Memory E	Bandwidth	381.4 GB/s		
# Nodes	Code 1	(A)	Code 2 (AD)
1 72		5.54	725.53	
8 7		9.58	7	9.64



Code Summary and Performance

Codes 1, 2, and 6 all show good scaling and similar performance

Code 5 uses ZERO directives

Code 6 uses 5.2x fewer directives than the original code, while Code 2 (within current spec) uses 2.7x fewer – with both exhibiting similar performance!

SUMMARY OF ALL MAS CODE VERSIONS DEVELOPED AND TESTED.				
Code Version	Code description and nvfortran GPU compiler flags	Total Lines	\$acc Lines	
0: CPU	Original CPU-only version	69874	Ø	
1: A	Original OpenACC implementation -acc=gpu -gpu=cc80	73865	1458	
2: AD	OpenACC for DC-incompatible loops and data management, DC for remaining loops -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged	71661	540	
3: ADU	OpenACC for DC-incompatible loops, DC for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80, managed	71269	162	
4: AD2XU	OpenACC for for functionality , DC2X for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80, managed	70868	55	
5: D2XU	<pre>DC2X for all loops, some code modifications, Unified memory -stdpar=gpu -gpu=cc80 -Minline=reshape,name:s2c, boost,interp,c2s,sv2cv</pre>	68994	Ø	
6: D2XAd	<pre>DC2X for all loops, some code modifications, OpenACC for data management -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged -Minline=reshape, name:s2c, boost, interp, c2s, sv2cv</pre>	71623	277	



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Performance Cont.

♥ Codes 3, 4, and 5 show poor performance and poor scaling – all use unified managed memory

They have ~25% lower performance with 1 GPU

With multiple GPUs over MPI (even on the same node) the performance is over 2x slower

WNVIDIA compiler developers are aware of this issue and working on a fix



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268.9	270.7_	273.0	
227.5	229.5	230.9	213.0 ₀
			183.5
CODE 3 CODE 4 CODE 5 CODE 6			



Performance Cont. Unified Managed Memory is not utilizing CUDA-aware MPI, resulting in a lot of CPU-GPU data transfers:



nsys profile --stats=true mpiexec -np 8 ./mas mas



NSIGHT SYSTEMS

MAS Production Code Implementation

Which version did we pick for our production code?

 Ψ Two code versions (both easy to maintain):

- Main code has minimal OpenACC directives so it can be compiled for GPUs using unified managed memory
 Lines: Total: 68,972 OpenACC: 132 (0.2%)
- "ACC" branch of code has OpenACC data movement added in; used in production releases Lines: Total: 70,658 OpenACC: 593 (0.8%)
- We have added OpenMP to OpenACC loops in ACC branch to allow hybrid-CPU mode
- W May convert OpenMP to OpenMP target off-load for future use with Intel GPUs





Summary and Future Outlook Do Concurrent in Fortran for accelerated computing

VISO standard (~0 chance of deprecation) Whore compact/simple code

 Ψ Computation loops exhibit similar performance to directives (when combined with directive manual data management)

 Ψ Currently supported by NVIDIA and Intel for their GPUs

 Ψ Lack of performance features (no async, no kernel fusion, no memory management) W Non-trivial performance drop for CUDA-aware MPI with NVIDIA (fix in progress) Ψ No current GPU DC support in GCC, AMD, Cray, Flang, etc. (some in progress...)

Still need OpenACC/OpenMP target for some time

Future Fortran language additions & compiler support for multi-vendor accelerators can lead to one code to run on them all



NVIDIA

AMD