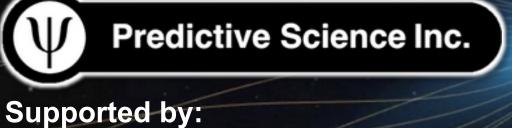
Acceleration of a production Solar MHD code with Fortran standard parallelism: From OpenACC to do concurrent

> Ronald M. Caplan, Miko M. Stulajter, and Jon A. Linker **Predictive Science Inc.** caplanr@predsci.com



# arXiv:2303.03398

# OpenACC WEBINAR **DIGITAL EVENT** JULY 11, 2023 1 PM EDT/10 AM PDT

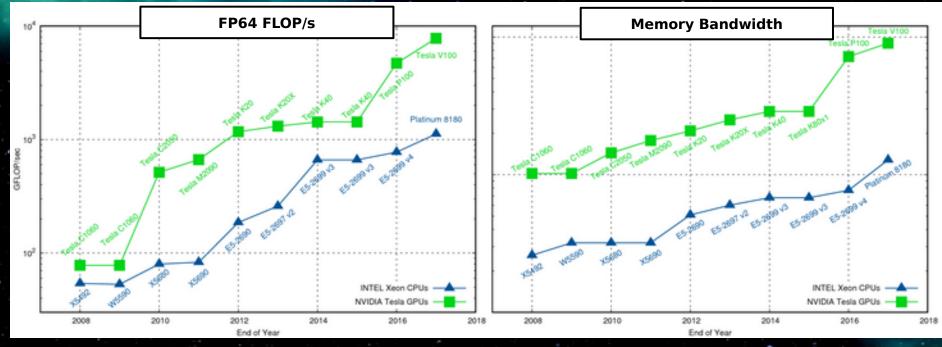
# Outline

Accelerated Computing Directives and Standard Parallelism Previous Implementations The MAS Code From OpenACC to Do Concurrent Performance Summary and Future Outlook



## Why Accelerated Computing?

- W Overall performance
  - FLOP/s
  - Memory Bandwidth
  - Specialized hardware
  - (e.g. ML/DL tensor cores)
- W Compact performance
  - In-house workstations
  - Reduce HPC real estate
  - Efficient performance Ψ
    - Lower energy use
    - Save money



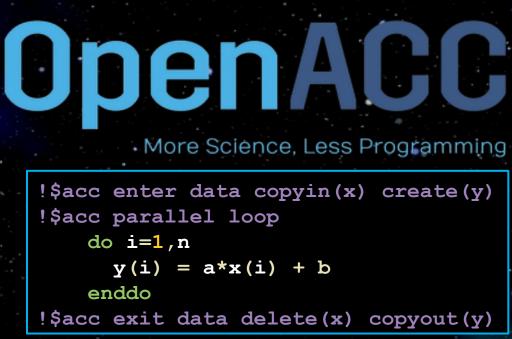






# Directives

- W Special comments that direct/allow the compiler to generate code that the base language does not support (e.g. parallelism, GPU-offload, data movement, etc.)
- Can produce single source code base for multiple (Ψ) targets (GPU, Multi-core CPU, FPGA, etc.)
- W Low-risk can ignore directives and compile as before
- W Vendor-independent (NVIDIA, AMD GCN, Intel, GCC, Cray, Flang, etc.)
- Great for rapid development and accelerating (Ψ) legacy codes
- W Two major directive APIs for accelerated computing: **OpenACC** and **OpenMP**





```
!$omp target enter data map(to:x) map(alloc:y)
$ somp target teams distribute parallel do
   do i=1, n
     y(i) = a * x(i) + b
   enddo
!$omp end target teams distribute parallel do
!$omp target exit data map(delete:x) map(from:y)
```

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## More Science, Less Programming

# !\$acc enter data copyin(x) create(y)

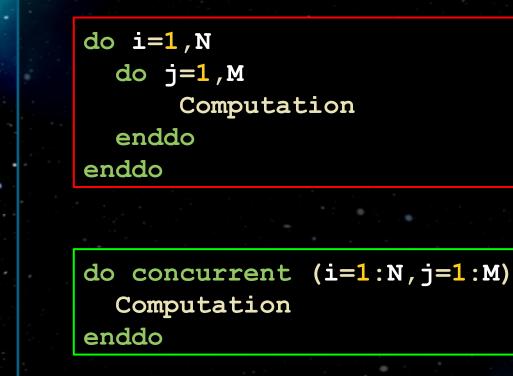
y(i) = a \* x(i) + b

### !\$acc exit data delete(x) copyout(y)

## Enabling HPC since 1997

# Fortran Standard Parallelism: Do Concurrent

- Introduced in ISO Standard Fortran 2008 (Ψ)
- Indicates loop can be run with **out-of-order** (Ψ) execution
- W Can be hint to the compiler that loop may be parallelizable
- W No current support for reductions, atomics, device selection, conditionals, etc.
- Fortran 202X (2023) specification will add reductions



-	1.1	Compiler	Version	DO CONCURRENT parallelization supp
18.13	(interest of the second	nvfortran	≥ 20.11	CPU and GPU with -stdpar
0.0.0	ortran	ifort/ifx	≥ 19.1 ≥ 23.0	CPU with -fopenmp CPU and GPU with -fopenmp-target-
0.8.0	accounts: gricolation tore	gfortran	≥9	<b>CPU with</b> -ftree-parallelize-loop

## s=<#Threads>

-do-concurrent

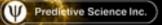
## port

## **Directives vs. Standard Parallelism**

Why use Fortran standard parallelism instead of directives?

- Understand (ISO)
- Use Lower code footprint
- W Less unfamiliar to domain scientists
- W For accelerated computing, directives are currently more portable (may change)

These reasons also apply to codes that already use directives



# Original Non-Parallelized Code

```
do k=1, np
  do j=1, nt
    do i=1,nrm1
      br(i,j,k) = (phi(i+1,j,k)-phi(i,j,k))*dr i(i)
    enddo
 enddo
enddo
```

!\$acc enter data copyin(phi,dr i) !\$acc enter data create(br) !\$acc parallel loop default(present) collapse(3) async(1) do k=1, np do j=1, ntdo i=1,nrm1 br(i,j,k) = (phi(i+1,j,k)-phi(i,j,k))\*dr i(i)enddo enddo enddo !\$acc wait !\$acc exit data delete(phi,dr i,br)

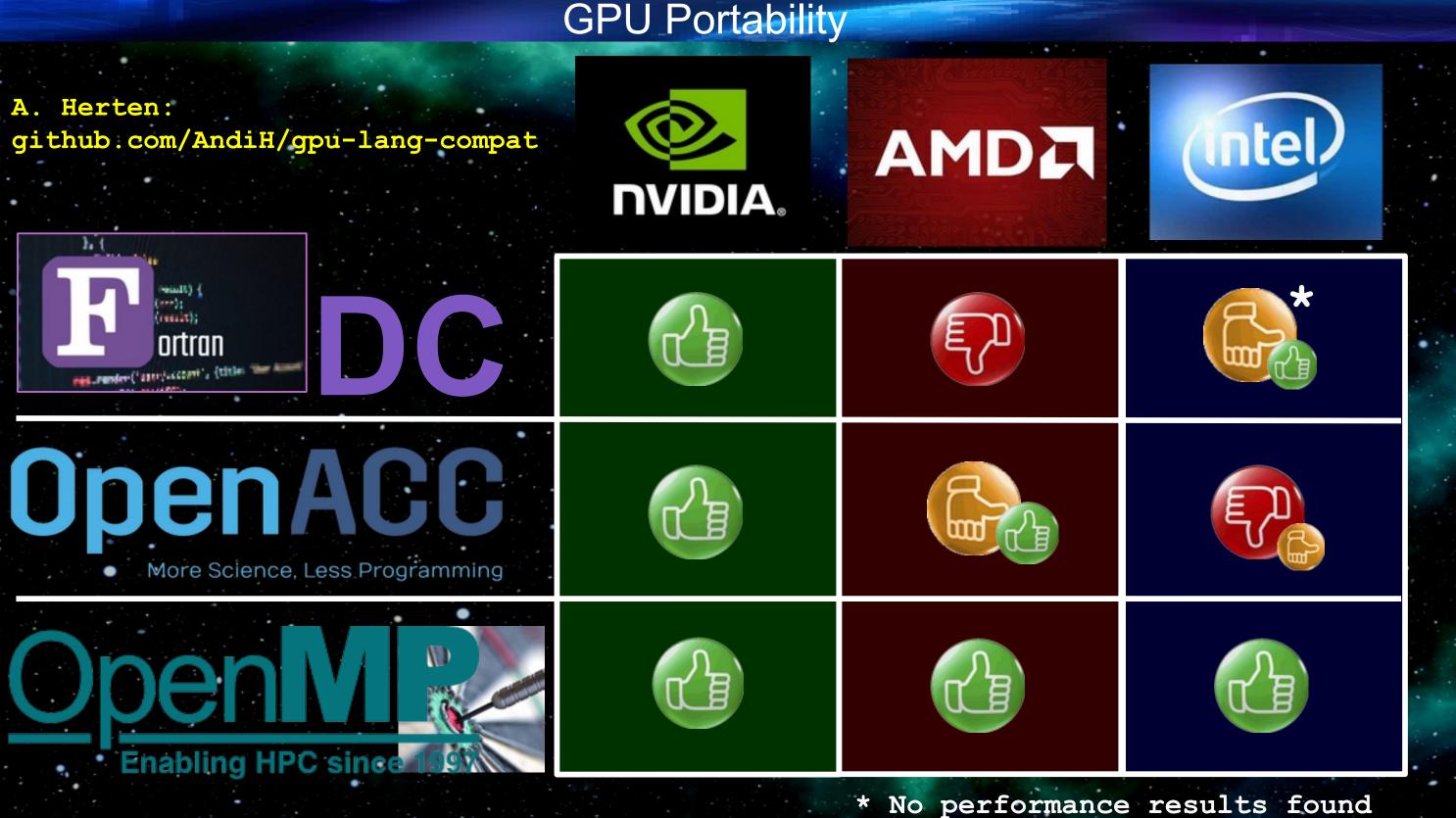
# Fortran's DO CONCURRENT

do concurrent (k=1:np,j=1:nt,i=1:nrm1) br(i,j,k) = (phi(i+1,j,k)-phi(i,j,k))\*dr i(i)enddo

# ized Code

### Herten: **A**. github.com/AndiH/gpu-lang-compat



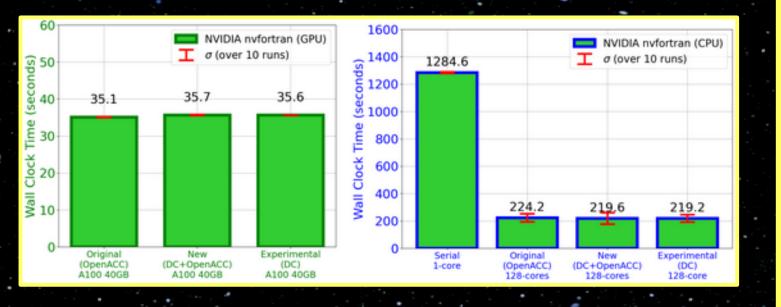


## **Previous Implementations**

W We have previously tested replacing OpenACC with DC in a small surface diffusion tool and in our medium-sized potential field solver code

The number of OpenACC directives were substantially or completely removed while (Ψ) maintaining similar performance

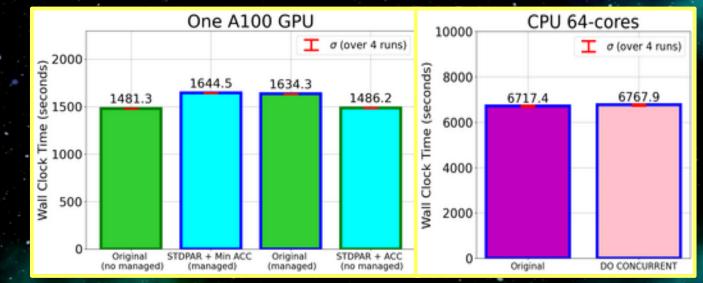
Stulajter, et. al. "Can Fortran's `do concurrent' Replace Directives for Accelerated Computing?" Lecture Notes in Computer Science, 13194, 3-21. Springer, Cham. (2021)





## github.com/predsci/POT3D

https://developer.nvidia.com/blog/using-fortranstandard-parallel-programming-for-gpu-acceleration



Here, we apply DC to our large-scale production code:



# The MAS Code



ALGORITHM OUTSIDE A SPHERE

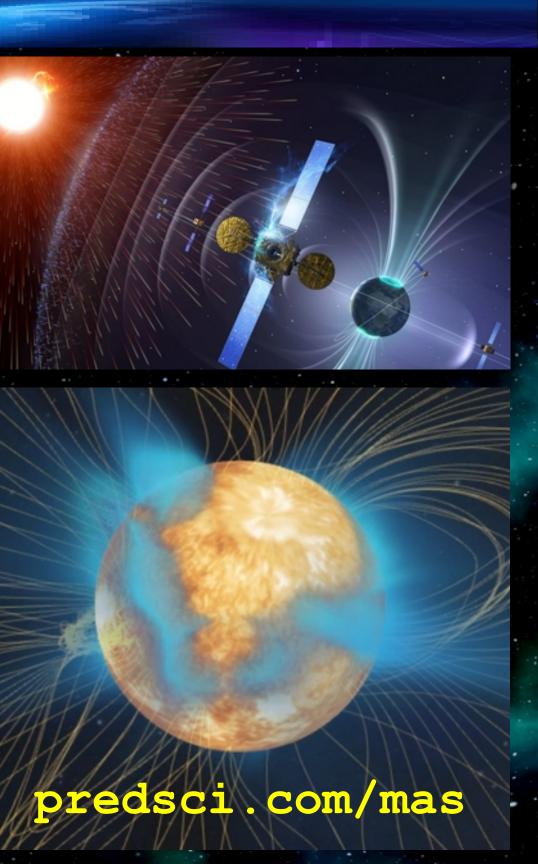
Purpose: General-purpose simulations of the corona and heliosphere for use with solar physics and space weather research

Model: Spherical 3D resistive thermodynamic MHD equations.

Algorithm: Implicit and explicit time-stepping with finite-difference stencils. Implicit steps use sparse matrix preconditioned iterative solver Highly memory bandwidth bound!

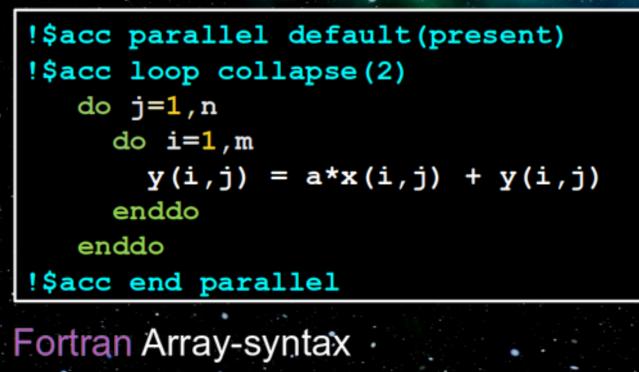
Code: ~70,000 lines of Fortran

Parallelism: MPI + OpenACC + (StdPar)

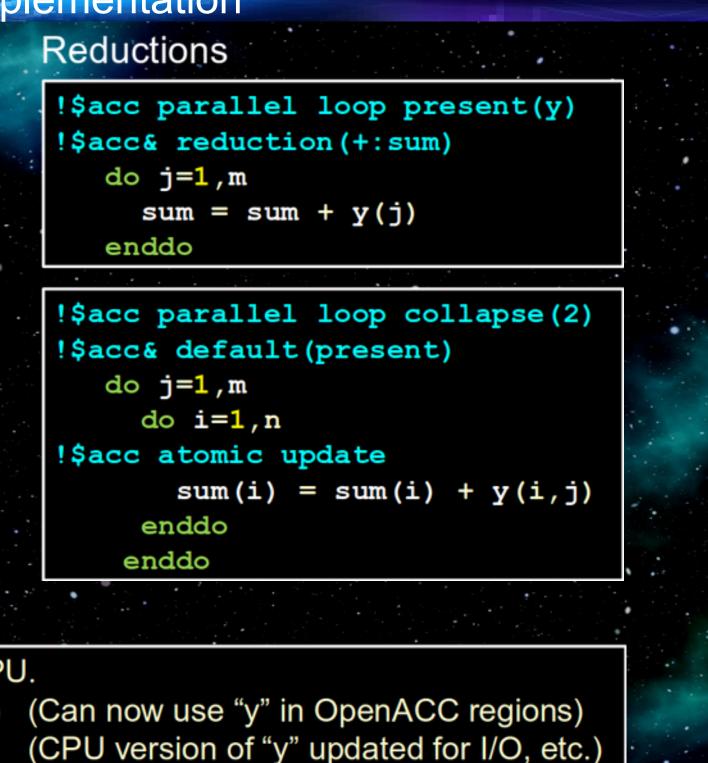


## MAS OpenACC Implementation

## **Basic Loop**



!\$acc kernels default(present)
 y(:,:) = a\*x(:,:) + y(:,:)
!\$acc end kernels





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## CPU↔GPU Data transfers

"y" is allocated and initialized on CPU. **!\$acc enter data copyin (y)** (Can now use "y" in OpenACC regions) **!\$acc update self (y)** (CPU version of "y" updated for I/O, etc. **!\$acc exit data delete(y)** (Free up GPU memory)

# MAS OpenACC Implementation Cont.

# Use multiple GPUs on one or more compute nodes



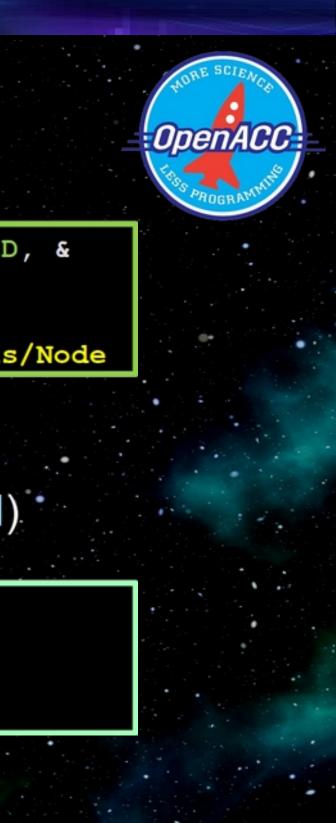
call MPI Comm split type (MPI COMM WORLD, MPI COMM TYPE SHARED, & 0, MPI INFO NULL, comm shared, ierr) call MPI Comm rank (comm shared, iprocsh, ierr) !\$acc set device num(iprocsh) !Assumes #GPUs/Node = #MPIranks/Node

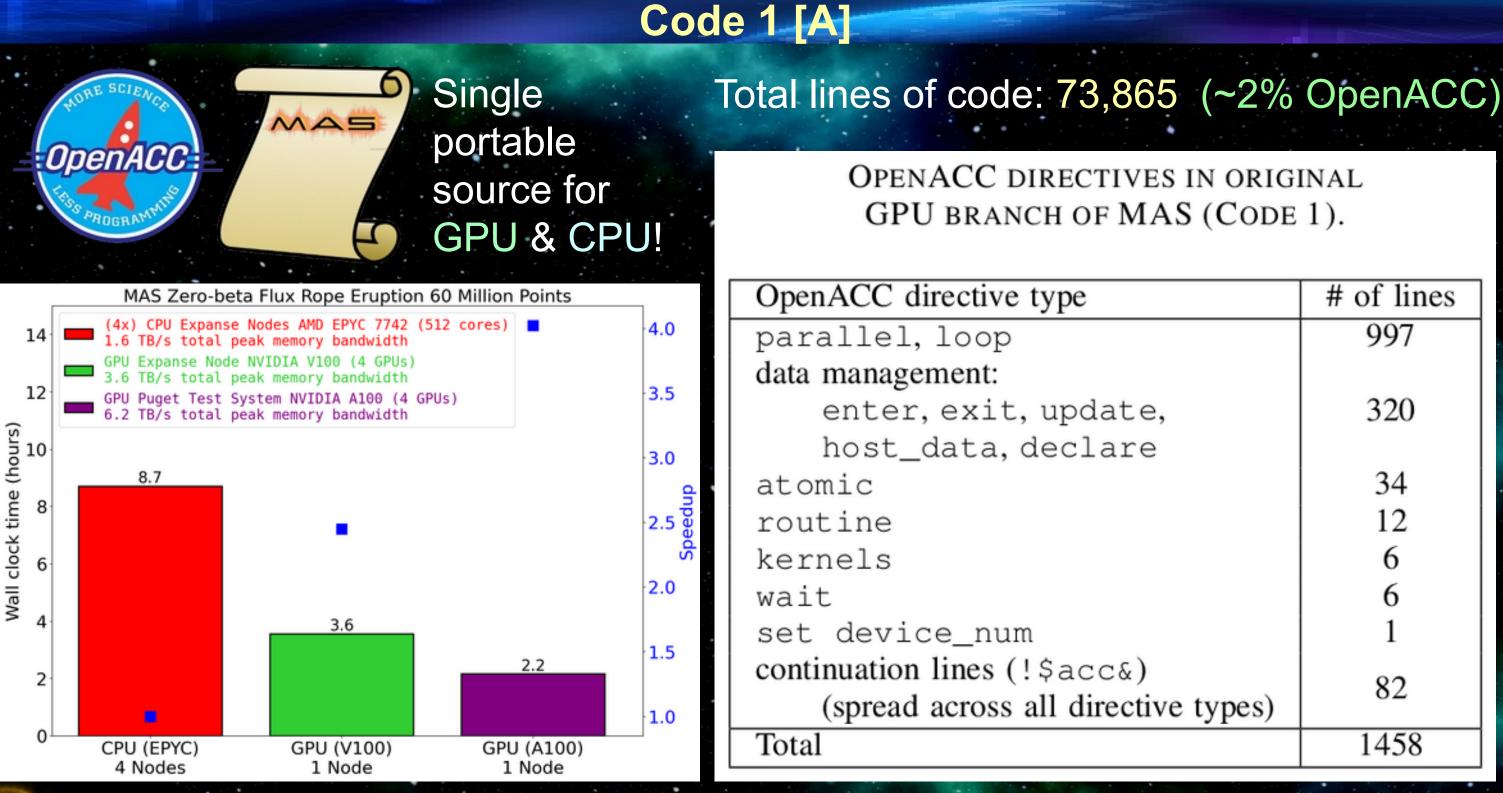
# Use GPU data directly with MPI calls (CUDA-aware MPI) \*

!\$acc host data use device(y) if present call MPI Allreduce (MPI IN PLACE, y, n, MPI DOUBLE, & MPI SUM, MPI COMM WORLD, ierr)

!\$acc end host data



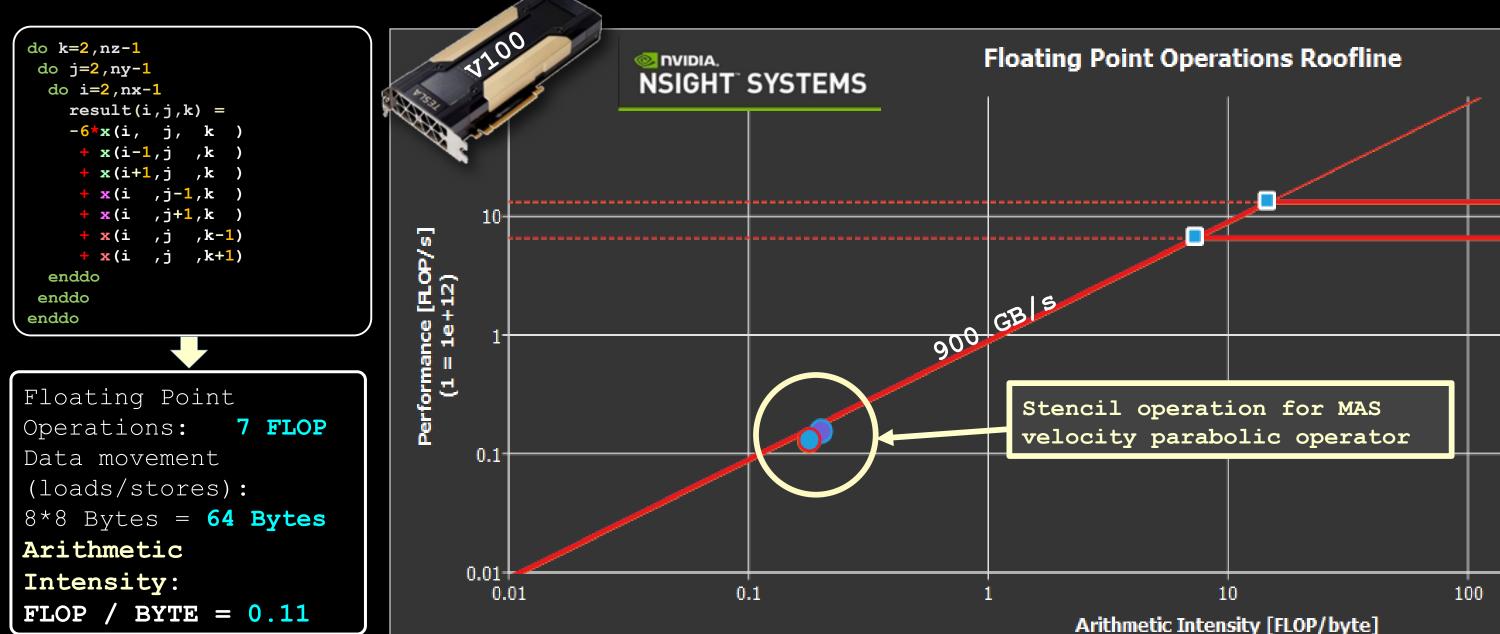




	# of lines
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	1458

## MAS OpenACC Implementation Cont: Performance Check

A roofline analysis shows how well given hardware is being utilized compared to the theoretical maximum for the given code







# MAS OpenACC to Do Concurrent

- W Multiple versions based on these considerations:
- W Avoid code refactoring (or not)
- W Adhere to ISO 2018 Fortran Standard (or not)
  - Data affinity statements (part of specification) not used as they are not currently supported by some compilers (e.g. GCC)

# W Using 202X preview & special features (or not)

- DC Reduction clause (nvfortran only)
- OpenACC directives within DC loops
- Use State Content of Content o
  - Unified managed memory vs. manual memory management

Code Version	Code description and nvfortran GPU compiler flags	Total Lines	\$ac Line
0: CPU	Original CPU-only version	69874	Ø
1: A	Original OpenACC implementation -acc=gpu -gpu=cc80	73865	145
2: AD	OpenACC for DC-incompatible loops and data management, DC for remaining loops -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged	71661	54(
3: ADU	OpenACC for DC-incompatible loops, DC for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80, managed	71269	16
4: AD2XU	OpenACC for for functionality , DC2X for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80, managed	70868	55
5: D2XU	DC2X for all loops, some code modifications, Unified memory -stdpar=gpu -gpu=cc80 -Minline=reshape,name:s2c, boost,interp,c2s,sv2cv	68994	Ø
6: D2XAd	DC2X for all loops, some code modifications, OpenACC for data management -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged -Minline=reshape, name:s2c, boost, interp, c2s, sv2cv	71623	277

SUMMARY OF ALL MAS CODE

/ERSIONS DEVELOPED AND TESTED.

# Code 2 [AD]

- W Start with Fortran 2018 specification compliance; no unified managed memory; no refactoring
- W No DC reduction support in current standard, so array reduction code would need refactoring

Functions/routines inside loops:

- DC requires they are "pure"
- Even so, nvfortran does not currently support them, so need OpenACC routine directives
- W Removing kernels used for array syntax and intrinsics (e.g. MINVAL) would need refactoring

```
!$acc parallel default(present)
!$acc loop collapse(2)
do j=1,n2
  do i=1,n1
!$acc atomic update
    sum0(i) = sum0(i) + array(i, j) * ...
  enddo
enddo
!$acc end parallel
```

module c2s\_interface !\$acc routine(c2s) seq interface pure subroutine c2s (x,y,z,r,t,p) use number types implicit none end subroutine c2s end interface end module

!\$acc kernels default(present) min\_field\_val\_local=MINVAL(field,mask) !\$acc end kernels

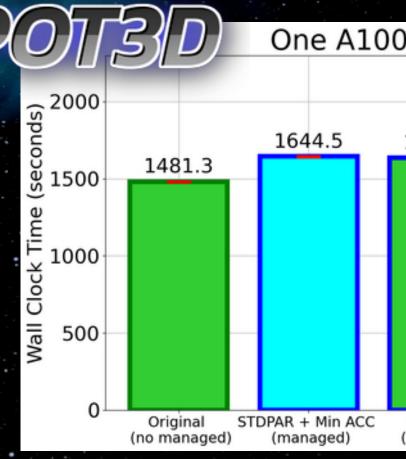
real(r\_typ), intent(in) :: x,y,z real(r\_typ), intent(out) :: r,t,p

# Code 2

Previous DC results show using unified managed memory (UM) can reduce performance, so we leave **OpenACC** data movement directives

W Kernel fusion (OpenACC parallel regions) and asynchronous computation (OpenACC async clause) are not available in DC

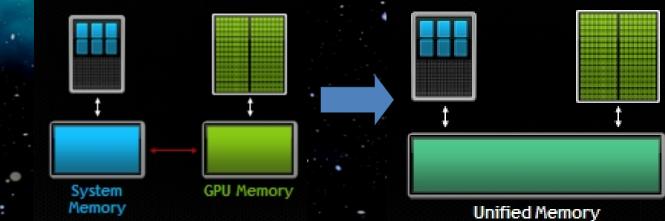
Code 2 [AD]: (Ψ) **OpenACC** for DC-incompatible loops and data management **DC** for all remaining loops

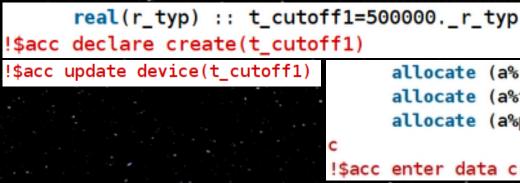


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Code	Code descrip	tion and		Total	\$acc
Version	nvfortran	GPU compi	ler flags	Lines	Lines
	Original Ope	nACC			
1: A	implementation	on		73865	1458
	-acc=qpu	-apu=cc8(	0		
	OpenACC for				
	loops and dat		ent,		
2: AD	DC for remai	ining loops		71661	540
	-acc=gpu	-			
	0855=uap-	, nomanage	ed		

# Code 3 [ADU]

- W Here, activate NVIDIA unified managed memory (UM) allowing removal of **OpenACC** data directives
- Can't remove all OpenACC data (Ψ) directives:
  - declare in function calls
  - Derived-type structures in OpenACC loops when using default (present)
- W Code 3 [ADU]: OpenACC for DC-incompatible loops, DC for all remaining loops, Unified managed memory





Code Version	Code description and nvfortran GPU compiler flags	Total Lines	\$acc Lines
2: AD	OpenACC for DC-incompatible loops and data management, DC for remaining loops -acc=gpu -stdpar=gpu	71661	540
3: ADU	OpenACC for DC-incompatible loops, DC for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80, managed	71269	162

## Developer View With Unified Memory

allocate (a%r(nrm1,nt,np)) allocate (a%t(nr,ntm1,np)) allocate (a%p(nr,nt,npm1))

### !\$acc enter data create(a)

# Code 4 [AD2XU]

- W Here, we use the Fortran 202X preview implementation in nvfortran
- DC reduction clause
- W No array reductions, but can use **OpenACC** atomics in DC loop
- W Able to remove most data clauses as all loops using derived types are now DC
- W Some OpenACC directives remain:
  - atomic, declare, update, set device num, routine, kernels
- **W** Code 4 **[AD2XU]**: **OpenACC** for functionality, DC 202X for all loops, Unified managed memory

do concurrent (k=2:npm1 reduce(+:sum0)) sum0=sum0+a(2,k)\*dph(k)\*pl\_1\*τwo enddo

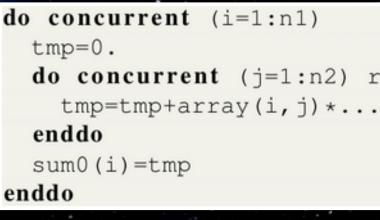
do concurrent (j=1:n2,i=1:n1) !\$acc atomic update sum0(i) = sum0(i) + array(i, j) \* ... enddo

Code	Code description and	Total	\$acc
Version 3: ADU	nvfortran GPU compiler flags OpenACC for DC-incompatible loops, DC for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80.managed	Lines 71269	Lines 162
4: AD2XU	OpenACC for for functionality , DC2X for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80,managed	70868	55

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# Code 5 [D2XU]

- W Here, we allow minor code refactoring W Replaced kernels with expanded DC loops W Array reduction loops modified to avoid atomic W Removed set device num by using BASH
  - launching script (OpenMPI-based) mpiexec -np <#> ./launch.sh ./mas
- W Use nvfortran flags to in-line routines, explicitly listing routines that can't be automatically in-lined
- Can eliminate duplicate CPU-only routing
- W Code 5 [D2XU]: DC 202X for all loops, Some code refactoring, Unified managed memory



launch.sh #!/bin/bash

# Execute code: exec \$\*

Code	Code description and	Total	\$acc
Version	nvfortran GPU compiler flags	Lines	Lines
4: AD2XU	OpenACC for for functionality , DC2X for remaining loops, Unified memory -acc=gpu -stdpar=gpu -gpu=cc80.managed	70868	55
5: D2XU	DC2X for all loops, some code modifications, Unified memory -stdpar=gpu -gpu=cc80 -Minline=reshape,name:s2c, boost,interp,c2s,sv2cv	68994	ø

**do concurrent** (j=1:n2) reduce(+:tmp)

Assume 1 GPU per MPI local rank Set device for this MPI rank: export CUDA\_VISIBLE\_DEVICES=" \$OMPI COMM WORLD LOCAL RANK"

# Code 6 [D2XAd]

Spoiler alert: Unified Managed Memory currently results in a nontrivial performance hit, especially across many MPI ranks

W Here, we take Code 5, but add back in (in minimal form) OpenACC data directives

Result is minimal number of directives, while retaining original performance

Code 6 [D2XAd]:
 DC 202X for all loops,
 Some code refactoring,
 OpenACC for data management

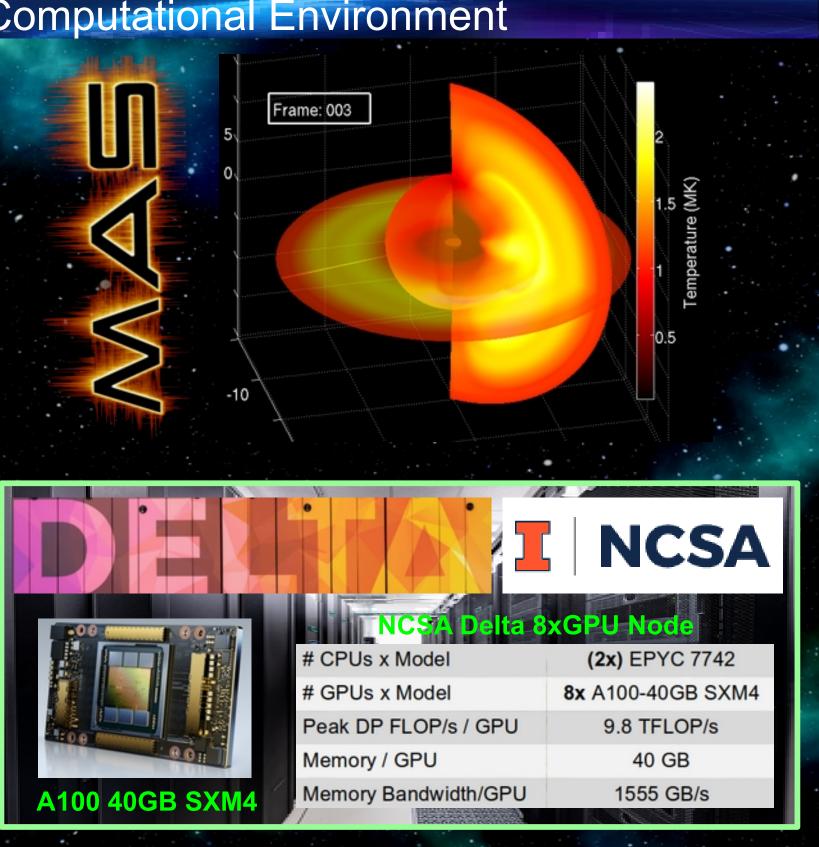


Code	Code description and	Total	\$acc
Version	nvfortran GPU compiler flags	Lines	Lines
5: D2XU	DC2X for all loops, some code modifications, Unified memory -stdpar=gpu -gpu=cc80 -Minline=reshape,name:s2c, boost_interp_c2s_sv2cv	68994	Ø
6: D2XAd	DC2X for all loops, some code modifications, OpenACC for data management -acc=gpu -stdpar=gpu -gpu=cc80, nomanaged -Minline=reshape, name:s2c, boost, interp, c2s, sv2cv	71623	277

# MAS Test Case and Computational Environment

- W Medium-sized production thermodynamic coronal relaxation
- W 36 million cells, 24 minutes physical time – Can fit on single 40GB GPU
- W DC has no effect on performance for CPU-only MPI runs:

		N.D.A.R.I.E.	SD	SC
# CPUs x Mode	el	(2x)	EPYC 7742	
# Total Cores		128	(we use 64)	
Peak FLOP/s		7.0 TFLOP/s		1EE
Memory		256 GB		ALL I
Total Memory E	Bandwidth	38	1.4 GB/s	115
			I THE REAL PROPERTY.	A COMPANY
# Nodes	Code 1	(A)	Code 2 (	AD)
1	725.54		725.53	
8	79.58		7	9.64
	and the second		11 Jacob	



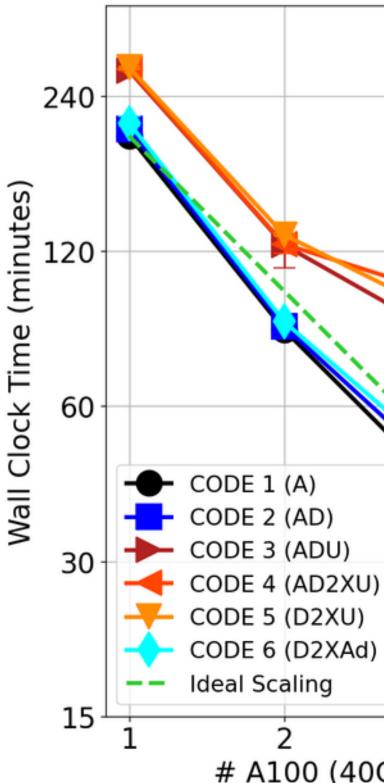
# **Code Summary and Performance**

Codes 1, 2, and 6 all show good scaling and similar performance

Code 5 uses ZERO directives

♥ Code 6 uses 5.2x fewer directives than the original code, while Code 2 (within current spec) uses 2.7x fewer – with both exhibiting similar performance!

SUMMARY OF ALL MAS CODE VERSIONS DEVELOPED AND TESTED.				
Code	Code description and	Total	\$acc	
Version	nvfortran GPU compiler flags	Lines	Lines	
0: CPU	Original CPU-only version	69874	Ø	
	Original OpenACC			
1: A	implementation	73865	1458	
	-acc=gpu -gpu=cc80			
	OpenACC for DC-incompatible			
	loops and data management,			
2: AD	DC for remaining loops	71661	540	
	-acc=gpu -stdpar=gpu			
	-gpu=cc80, nomanaged			
	OpenACC for DC-incompatible			
2 1 5 1	loops, DC for remaining loops,	712(0	162	
3: ADU	Unified memory	71269		
	-acc=gpu -stdpar=gpu			
	-gpu=cc80, managed			
	OpenACC for for functionality			
4. ADOVIL	, DC2X for remaining loops,	70969		
4: AD2XU	Unified memory	70868	55	
	-acc=gpu -stdpar=gpu			
	-gpu=cc80, managed DC2X for all loops,			
	some code modifications,			
	Unified memory		~	
5: D2XU	-stdpar=gpu -gpu=cc80	68994	Ø	
	-Minline=reshape, name:s2c,			
	boost, interp, c2s, sv2cv			
	DC2X for all loops,			
	some code modifications,			
	OpenACC for data management			
6: D2XAd	-acc=gpu -stdpar=gpu	71623	277	
	-gpu=cc80, nomanaged			
	-Minline=reshape, name:s2c,			
	boost, interp, c2s, sv2cv			



# 8 # A100 (40GB) GPUs

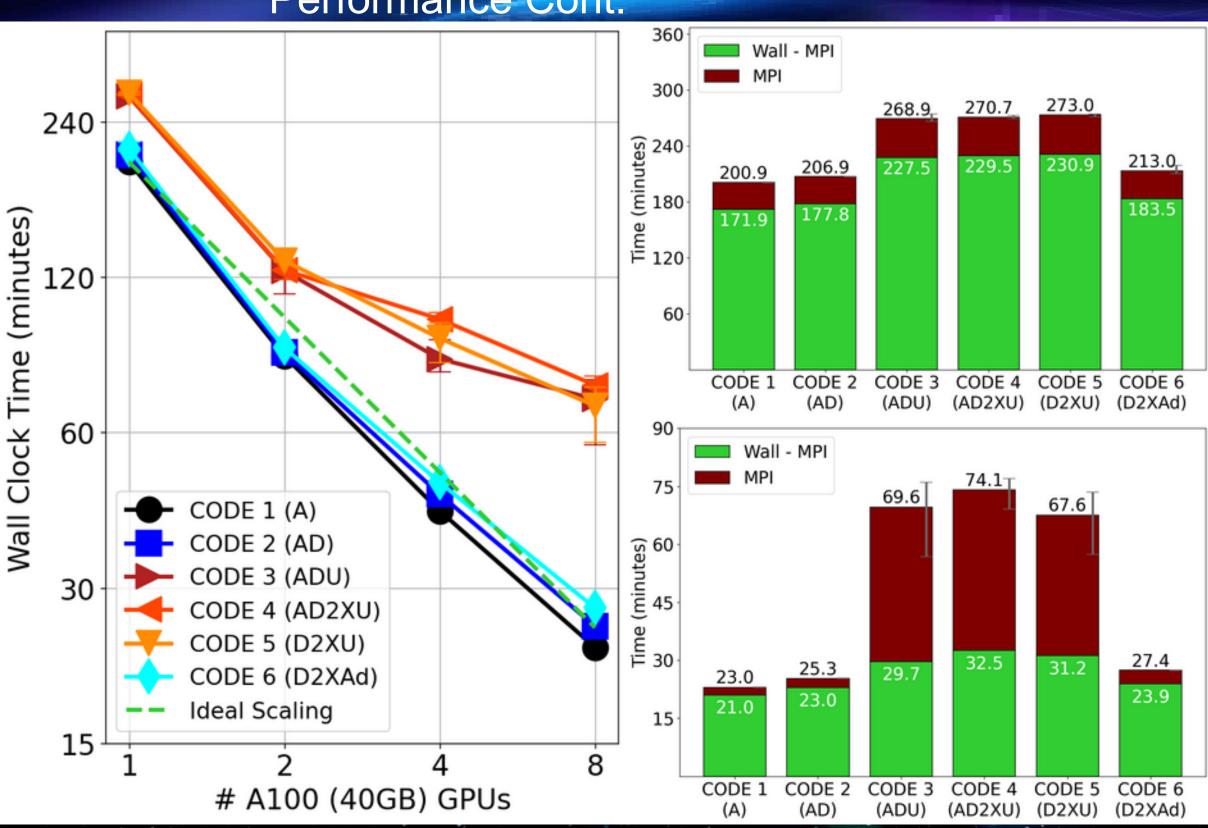
## Performance Cont.

••• Codes 3, 4, and 5 show poor performance and poor scaling – all use unified managed memory

♥ They have ~25% lower performance with 1 GPU

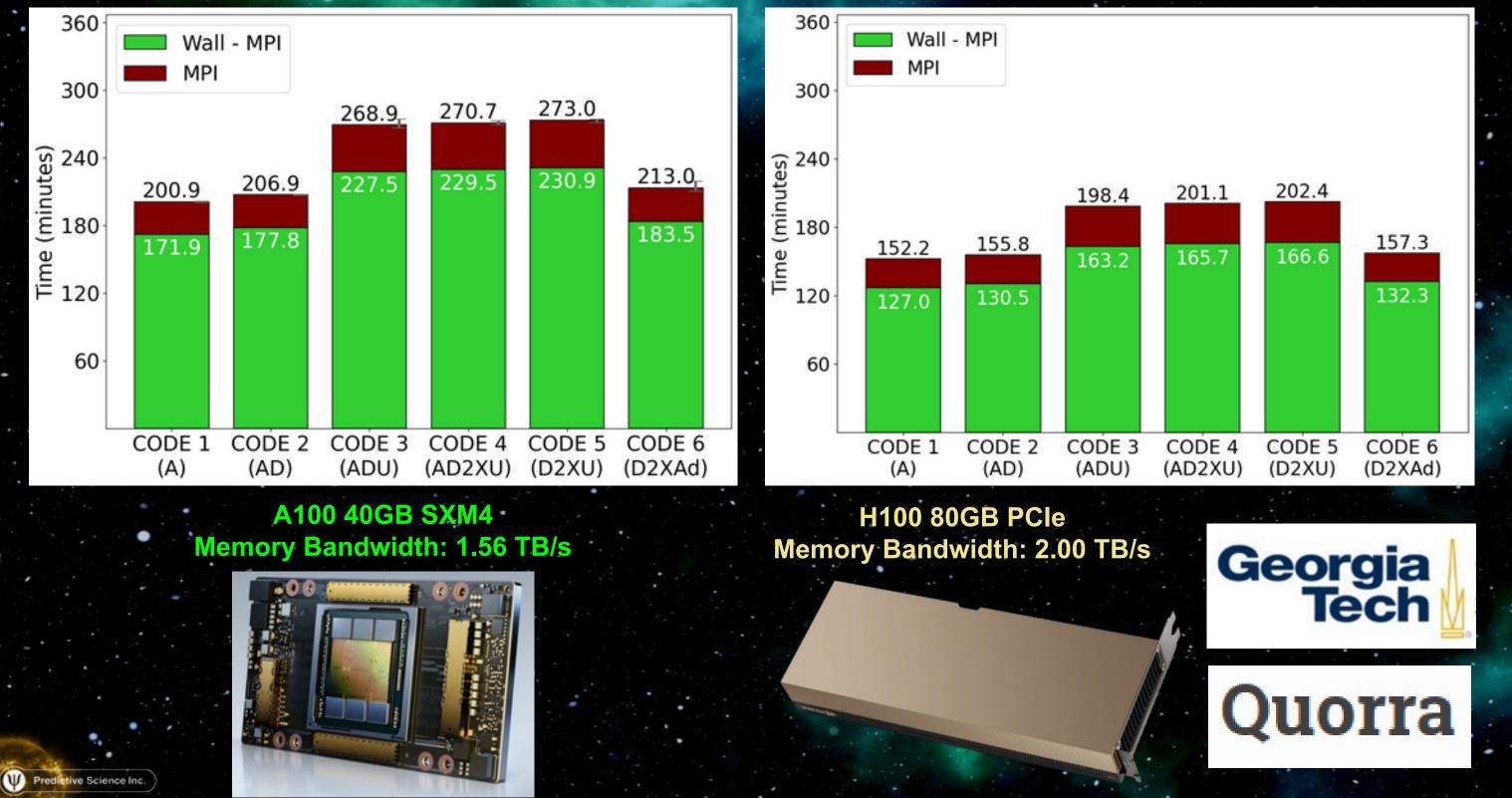
With multiple GPUs over MPI (even on the same node) the performance is over 2x slower

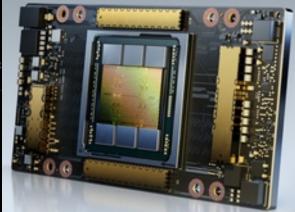
**WNVIDIA** compiler developers are aware of this issue



268.9 <sub>5</sub>	270.7	273.0	
227.5	229.5	230.9	213.0 <sub>r</sub>
			183.5
CODE 3 (ADU)	CODE 4 (AD2XU)		

## Performance Cont.





# Performance Cont. W Unified Managed Memory is not utilizing CUDA-aware MPI, resulting in a lot of CPU-GPU data transfers:



nsys profile --stats=true mpiexec -np 8 ./mas mas

23s - +959ms +959.5ms +960m	ms +960.5ms +961ms +961.5ms +962ms +962.5ms +963.5ms +963.5ms +964ms +964.5ms +965ms +965.5ms +966ms	
> CPU (128)		
- Processes (20)	One solver iteration	
• [2362912] ./mas		
• [2362910] ./mas		
- Threads (10)		
• 👽 [2362911] mas •		
OS runtime librarles		
CUDA API	r o.st o.str o.str o.str o.str o.str	ze cuStr
Profiler overhead	GPU peer-to-peer data transfers	
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- CUDA HW (0000:8b:00.0 - NVIDIA A100-SXM4-40GB)	an, and an a sub- , and a sub- , a sub- , a sub-	
All Streams)     All Streams)	c. (gao. arp.)	911_gpu (g.,
	Code 2 [AD]	
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> CPU (128)	One solver iteration	
- Processes (20)	One solver iteration	
• [1049943] ./mas		
- [1049946] ./mas     - Threads (10)		
• 🕼 [1049946] mas •		
CUDA API		cuStreamSynchronize
	NSE: 0.5.: 0.5tream5y.: 0.5trea.: 0.65tre C., C., C., C., C., C., C., C., C.,	custreamsynchronize
Profiler overhead	GPU-CPU data transfers 🥿	
9 threads hidden+		
- 94.6% Context 1		
(All Streams)	Me., Mem., Memcpy DtoH Memcpy Memc., Mem. Mem. Mem. Mem., Me	minus_div_grad_v_28911_
	Code 3 [ADU]	

## 📀 NVIDIA. **NSIGHT** SYSTEMS

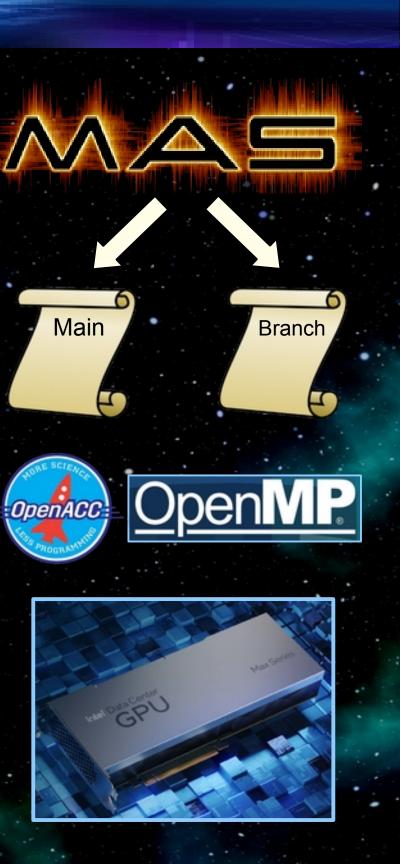


## MAS Production Code Implementation

Which version did we pick for our production code?

W Two code versions (both easy to maintain):

- Main code has minimal OpenACC directives so it can be compiled for GPUs using unified managed memory
   Lines: Total: 68,972 OpenACC: 132 (0.2%)
- "ACC" branch of code has OpenACC data movement added in; used in production releases
   Lines: Total: 70,658 OpenACC: 593 (0.8%)
- We have added OpenMP to OpenACC loops in ACC branch to allow hybrid-CPU mode
- W May convert OpenMP to OpenMP target off-load for future use with Intel GPUs



# Summary and Future Outlook Do Concurrent in Fortran for accelerated computing

**WISO standard** (~0 chance of deprecation)

W More compact/simple code

Computation loops exhibit similar performance to directives (when combined with directive manual data management)

Can add hybrid MPI+thread CPU parallelism
 Currently supported by NVIDIA and Intel for their GPUs

U Lack of performance features (no async, no kernel fusion, no memory management)
 W Non-trivial performance drop for CUDA-aware MPI with NVIDIA (fix in progress)
 W No current GPU DC support in GCC, AMD, Cray, Flang, etc. (some in progress...)

W Still need OpenACC/OpenMP target for some time

Future Fortran language additions & compiler support for multi-vendor accelerators can lead to one code to with on them all.

